

WHAT IS CLAIMED IS:

- 1           1.     A program storage device readable by a computer, the program storage  
2     device tangibly embodying one or more programs of instructions executable by the  
3     computer to perform operations for determining when to perform an error recovery  
4     instruction, the operations comprising:  
5         receiving an error recovery instruction;  
6         beginning a timeout task;  
7         monitoring processor status to determine a time to perform the error recovery  
8     instruction; and  
9         performing the error recovery instruction when the monitoring determines a  
10    time for performing the error recovery.
  
- 1           2.     The program storage device of claim 1 further comprising forcing an  
2     execution of the error recovery instruction when the timeout task expires before the  
3     monitoring determines a time to perform the error recovery instruction.
  
- 1           3.     The program storage device of claim 2 further comprising resuming  
2     normal operations after performing the error recovery instruction.

1           4.       The program storage device of claim 1, wherein the monitoring  
2   processor status to determine a time to perform the error recovery instruction further  
3   comprises:  
4           monitoring a processor interface for an idle condition;  
5           withholding access to the processor interface when the idle condition is  
6   detected;  
7           after access to the processor interface is withheld, interrogating all data transfer  
8   paths to determine when all the data paths are idle; and  
9           identifying the time to perform the error recovery instruction when all data  
10   transfer paths are idle.

1           5.       The program storage device of claim 4 further comprising resuming  
2   normal operations after performing the error recovery instruction.

1           6.       The program storage device of claim 1 further comprising resuming  
2   normal operations after performing the error recovery instruction.

1           7.     A program storage device readable by a computer, the program storage  
2 device tangibly embodying one or more programs of instructions executable by the  
3 computer to perform operations for determining when to perform an error recovery  
4 instruction, the operations comprising:  
5           receiving an error recovery instruction;  
6           monitoring processor status to determine a time to perform the error recovery  
7 instruction; and  
8           performing the error recovery instruction when the monitoring determines a  
9 time for performing the error recovery.

1           8.     The program storage device of claim 7 further comprising beginning a  
2 timeout task after receiving the error recovery instruction and forcing an execution of  
3 the error recovery instruction when the timeout task expires before the monitoring  
4 determines a time to perform the error recovery instruction.

1           9.     The program storage device of claim 8 further comprising resuming  
2 normal operations after performing the error recovery instruction.

1           10.     The program storage device of claim 7, wherein the monitoring  
2     processor status to determine a time to perform the error recovery instruction further  
3     comprises:  
4           monitoring a processor interface for an idle condition;  
5           withholding access to the processor interface when the idle condition is  
6     detected;  
7           after access to the processor interface is withheld, interrogating all data transfer  
8     paths to determine when all the data paths are idle; and  
9           identifying the time to perform the error recovery instruction when all data  
10    transfer paths are idle.

1           11.     The program storage device of claim 10 further comprising resuming  
2     normal operations after performing the error recovery instruction.

1           12.     The program storage device of claim 7 further comprising resuming  
2     normal operations after performing the error recovery instruction.

1           13.     An apparatus for quiescing processor control logic upon receipt of an  
2 error recovery instruction, comprising:  
3           self-quiesce logic, coupled to the timer, the self-quiesce logic receiving an error  
4 recovery instruction; and  
5           a timer for determining when to force execution of the error recovery  
6 instruction;  
7           wherein the self-quiesce logic initiates the timer when the error recovery  
8 instruction is received, begins to monitor processor status to determine a time to  
9 perform the error recovery instruction and performs the error recovery instruction when  
10 the monitoring determines a time for performing the error recovery.

1           14.     The apparatus of claim 13, wherein the self-quiesce logic forces an  
2 execution of the error recovery instruction when the timer expires before the self-  
3 quiesce logic determines a time to perform the error recovery instruction.

1           15.     The apparatus of claim 14, wherein the self-quiesce logic allows  
2 resuming normal operations after the error recovery instruction is performed.

1           16.     The apparatus of claim 13, wherein the self-quiesce logic monitors  
2     processor status to determine a time to perform the error recovery instruction by  
3     monitoring a processor interface for an idle condition, withholding access to the  
4     processor interface when the idle condition is detected, after access to the processor  
5     interface is withheld, interrogating all data transfer paths to determine when all the data  
6     paths are idle and identifying the time to perform the error recovery instruction when  
7     all data transfer paths are idle.

1           17.     The apparatus of claim 16, wherein the self-quiesce logic allows  
2     resuming normal operations after the error recovery instruction is performed.

1           18.     The apparatus of claim 13, wherein the self-quiesce logic allows  
2     resuming normal operations after the error recovery instruction is performed.

1           19.     An apparatus for quiescing processor control logic upon receipt of an  
2     error recovery instruction, comprising:  
3             a processor for executing instructions; and  
4             self-quiesce logic, coupled to the processor, the self-quiesce logic detecting an  
5     error recovery instruction, wherein the self-quiesce logic monitors processor status to  
6     determine a time to perform the error recovery instruction and performs the error  
7     recovery instruction when the monitoring determines a time for performing the error  
8     recovery.

1           20.     The apparatus of claim 19 further comprising a timer for determining  
2     when to abort the monitoring of processor status and data path activity and cause an  
3     execution of the error recovery instruction.

1           21.     The apparatus of claim 20, wherein the self-quiesce logic causes normal  
2     operations to be resumed after performing the error recovery instruction.

1           22.     The apparatus of claim 19, wherein the self-quiesce logic monitors  
2     processor status to determine a time to perform the error recovery instruction by  
3     monitoring a processor interface for an idle condition, withholding access to the  
4     processor interface when the idle condition is detected, after access to the processor  
5     interface is withheld, interrogating all data transfer paths to determine when all the data  
6     paths are idle and identifying the time to perform the error recovery instruction when  
7     all data transfer paths are idle.

1           23.     The apparatus of claim 22, wherein the self-quiesce logic causes normal  
2     operations to be resumed after performing the error recovery instruction.

1           24.     The apparatus of claim 19, wherein the self-quiesce logic causes normal  
2     operations to be resumed after performing the error recovery instruction.

1           25.     A method for determining when to perform an error recovery  
2     instruction, comprising:  
3           receiving an error recovery instruction;  
4           beginning a timeout task;  
5           monitoring processor status to determine a time to perform the error recovery  
6     instruction; and  
7           performing the error recovery instruction when the monitoring determines a  
8     time for performing the error recovery.

1           26.     A method for determining when to perform an error recovery  
2     instruction, comprising:  
3           receiving an error recovery instruction;  
4           monitoring processor status to determine a time to perform the error recovery  
5     instruction; and  
6           performing the error recovery instruction when the monitoring determines a  
7     time for performing the error recovery.



1           27.     An apparatus for quiescing processor control logic upon receipt of an  
2 error recovery instruction, comprising:  
3           means for receiving an error recovery instruction; and  
4           means for determining when to force execution of the error recovery instruction;  
5           wherein the means for receiving the error recovery instruction initiates the timer  
6 when the error recovery instruction is received, begins to monitor processor status to  
7 determine a time to perform the error recovery instruction and performs the error  
8 recovery instruction when a time for performing the error recovery is determined.

1           28.     An apparatus for quiescing processor control logic upon receipt of an  
2 error recovery instruction, comprising:  
3           means for executing instructions; and  
4           means, coupled to the means for executing instructions, for detecting an error  
5 recovery instruction, monitoring processor status to determine a time to perform the  
6 error recovery instruction and performing the error recovery instruction when a time for  
7 performing the error recovery is determined.